REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change package designation and add case outline figure. - jak	00-04-11	Monica L. Poelking
B	Add device type 02. - jak	00-05-30	Monica L. Poelking
C	Correct supply voltage nomenclature to comply with device characterization. Correct dimension A minimum values for case outline X in table of figure 1. Update boilerplate to latest MIL-PRF-38535 requirements. - CFS	01-03-06	Thomas M. Hess
D	Add device type 03. - CFS	02-05-10	Thomas M. Hess
E	Add device types 04 and 05. Change load capacitance value for AC tests and add output skew to table IA. Update boilerplate. Editorial changes throughout. - LTG	04-07-29	Thomas M. Hess
F	Add device types 06 and 07. Add figure A-2 to appendix A. Update radiation hardness assurance requirements. - LTG	07-06-27	Thomas M. Hess
G	Correct the input voltage range specified in paragraph 1.4. - CFS	08-05-05	Thomas M. Hess
H	Add new device number 08. Add case outline Y for device type 08 in section 1.2.4. - MAA	09-10-05	Thomas M. Hess
J	To add footnotes 21/ and 22/ for t_{SKEW} and t_{DSKEW} for device types 01 to 07 in table IA. Update radiation features in section 1.5 and SEP test limit table IB. - MAA	10-12-20	Thomas M. Hess
K	Add equivalent test circuits and footnote 5 to figure 5. Delete class M requirements per updated boilerplate paragraphs. - MAA	12-12-10	Thomas M. Hess
L	Add class Q level device type 08. Update recommended input voltage (V_{IN}) range in section 1.4. - MAA	14-03-10	Thomas M. Hess

REV																				
SHEET																				
REV	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L					
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49					
REV	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS															
REV	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
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DRAWING APPROVAL DATE
99-05-10

REVISION LEVEL
L

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

MICROCIRCUIT, DIGITAL, RADIATION HARDENED, ADVANCED CMOS, SCHMITT 16-BIT BIDIRECTIONAL MULTI-PURPOSE TRANSCEIVER WITH THREE-STATE OUTPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-98580**

SHEET 1 OF 49

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	R	98580	01	V	X	X
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)
Drawing number						

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACS164245S	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs and cold sparing
02	54ACS164245S 1/	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs, cold sparing, and extended voltage range
03	54ACS164245S 1/ 2/	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs, cold sparing, extended voltage range, and extended industrial temperature range of -40°C to +125°C
04	54ACS164245SE 1/	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs, cold sparing, extended voltage range, and enhanced AC's
05	54ACS164245SE 1/ 2/	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs, cold sparing, extended voltage range, extended industrial temperature range of -40°C to +125°C, and enhanced AC's
06	54ACS164245SEI 1/	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs, cold sparing, warm sparing, extended voltage range, enhanced AC's and improved power management
07	54ACS164245SEI 1/ 2/	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs, cold sparing, warm sparing, extended voltage range, industrial temperature range of -40°C to +125°C, enhanced AC's and improved power management
08	54ACS164245	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs and cold sparing.

1/ Device types 02, 03, 04, 05, 06, and 07 have an extended voltage range.
2/ Device types 03, 05, and 07 have an extended industrial temperature range of -40°C to +125°C.

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	48	Flat pack
Y	See figure 1	48	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage ranges (V_{DD}):
- 5.0 V supply (V_{DD1}) .... -0.3 V dc to +6.0 V dc
- 3.3 V supply (V_{DD2}) .... -0.3 V dc to +6.0 V dc

DC input voltage range (V_{IN}): 4/
- A port .... -0.3 V dc to V_{DD1} + 0.3 V dc
- B port .... -0.3 V dc to V_{DD1} + 0.3 V dc

DC output voltage range (V_{OUT}):
- A port .... -0.3 V dc to V_{DD1} + 0.3 V dc
- B port .... -0.3 V dc to V_{DD1} + 0.3 V dc

DC input current, any one input (I_{IN}):
- A port .... ±10 mA
- B port .... ±10 mA

Storage temperature range (T_{STG}) .... -65°C to +150°C
Lead temperature (soldering, 10 seconds) .... +300°C
Thermal resistance, junction-to-case (θ_{JC}) .... See MIL-STD-1835
Junction temperature (T_J) .... +175°C
Maximum power dissipation at T_A = +55°C (in still air) (P_D) .... 1.0 W 5/

See footnotes on next sheet.

1.4 Recommended operating conditions. 2/ 3/ 6/

Supply voltage range (V_{DD}):
Device type 01 (V_{DD1}).. +4.5 V dc to +5.5 V dc or 3.13 V dc to 3.6 V dc
Device types 02, 03, 04, 05, 06, and 07 (V_{DD1}) .... +4.5 V dc to +5.5 V dc or 3.0 V dc to 3.6 V dc
Device type 08 (V_{DD1}).. +4.5 V dc to +5.5 V dc or 2.3 V dc to 3.6 V dc
Device type 01 (V_{DD2}).. +3.13 V dc to +3.6 V dc or +4.5 V dc to +5.5 V dc
Device types 02, 03, 04, 05, 06, and 07 (V_{DD2}) .... +3.0 V dc to +3.6 V dc or +4.5 V dc to +5.5 V dc
Device type 08 (V_{DD2}).. +2.3 V dc to +3.6 V dc or +4.5 V dc to +5.5 V dc
Input voltage range (V_{IN}):
A port (for device 01 to 07)... +0.0 V dc to V_{DD2}
B port (for device 01 to 07)... +0.0 V dc to V_{DD1}
A port (for device 08) .... +0.0 V dc to V_{DD1}
B port (for device 08) .... +0.0 V dc to V_{DD1}
Control inputs ($\overline{OE}1$, $\overline{OE}2$, DIR1, DIR2) (for device 01 to 07).............................. +0.0 V dc to V_{DD1}
Output voltage range (V_{OUT})... +0.0 V dc to V_{DD1}
Case operating temperature range (T_C):
Device types 01, 02, 04, 06 and 08 .... -55°C to +125°C
Device types 03, 05, and 07 .... -40°C to +125°C
Maximum input rise or fall time rate ($\Delta t/\Delta V$):
at V_{DD1} = 4.5 V (for device 01 to 07) .... 1 ns/V 7/
Maximum input rise or fall time rate ($\Delta t/\Delta V$):
at V_{CC} = 3.0, 4.5 or 5.5 V (for device 08) .... 0 to 8 ns/V 7/

1.5 Radiation features. 8/

Maximum total dose available (dose rate = 50 - 300 rad (Si)/s) .... 100 Krad (Si)
Single event phenomenon (SEP) :
Effective LET, no upsets (SEU) (see 4.4.4.4)
for device types 01 to 07 .... ≤ 80 MeV/(mg/cm^2)
for device type 08 .... ≤ 64 MeV/(mg/cm^2)
Effective LET , no latch-up (SEL) (see 4.4.4.4)
for device types 01-05 .... ≤ 120 MeV/(mg/cm^2)
for device types 06-07 .... ≤ 114 MeV/(mg/cm^2)
for device type 08 .... ≤ 111 MeV/(mg/cm^2)

____

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to V_{SS}.
3/ The limits for the parameters specified herein shall apply over the full specified V_{DD} range and case temperature range of -55°C to +125°C for device types 01, 02, 04, 06 and, 08; and -40°C to +125°C for device types 03, 05 and 07.
4/ For cold spare mode (V_{DD} = V_{SS}), V_{IN} may be –0.3 V to the maximum recommended operating V_{DD} + 0.3 V.
5/ The maximum package power dissipation is calculated by using a junction temperature of 150°C, a board trace length of 750 mils and thermal resistance, junction-to-air ambient (θ_{JA}) is 95°C/W.
6/ Unused inputs must be held high or low to prevent them from floating.
7/ Derate system propagation delays by difference in rise time to switch point for t_r or t_f > 1 ns/V.
8/ Radiation testing is performed on the standard evaluation circuit.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at http://www.astm.org/ or from ASTM International, P. O. Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959).

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC JESD 78 – IC Latch-Up Test

(Copies of these documents are available online at http://www.jedec.org/ or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535, and as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.2.6 Irradiation test connections. The irradiation test connections shall be as specified in table III.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535, shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ 2/ 3/ $-55°C \leq T_C \leq +125°C$ For 5.0 V supply: $+4.5\ V \leq V_{DD1} \leq +5.5\ V$ For 3.3 V supply: $+3.0\ V \leq V_{DD2} \leq +3.6\ V$ unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/		Unit
						Min	Max	
Schmitt trigger positive going	V_{T+}	A Port = 3.3 V	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3		$0.7V_{DD2}$	V
		A Port = 3.3 V	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3		$0.7V_{DD2}$	
		A Port = 3.3 V	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 2.7 V and 3.6 V	1, 2, 3		$0.7V_{DD2}$	
		A Port = 5.0 V	All	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	1, 2, 3		$0.7V_{DD2}$	
		B Port = 3.3 V	01	V_{DD1} = 3.13 V and 3.6 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3		$0.7V_{DD1}$	
		B Port = 3.3 V	02, 03, 04, 05, 06, 07	V_{DD1} = 3.0 V and 3.6 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3		$0.7V_{DD1}$	
		B Port = 3.3 V	08	V_{DD1} = 2.7 V and 3.6 V, V_{DD2} = 2.7 V and 3.6 V	1, 2, 3		$0.7V_{DD1}$	
		B Port = 5.0 V	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3		$0.7V_{DD1}$	
		B Port = 5.0 V	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3		$0.7V_{DD1}$	
		B Port = 5.0 V	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 2.7 V and 3.6 V	1, 2, 3		$0.7V_{DD1}$	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ 2/ 3/ $-55°C \leq T_C \leq +125°C$ For 5.0 V supply: $+4.5 V \leq V_{DD1} \leq +5.5 V$ For 3.3 V supply: $+3.0 V \leq V_{DD2} \leq +3.6 V$ unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/		Unit
						Min	Max	
Schmitt trigger negative going	V_{T-}	A Port = 3.3 V	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3	$0.3V_{DD2}$		V
		A Port = 3.3 V	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3	$0.3V_{DD2}$		
		A Port = 3.3 V	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 2.7 V and 3.6 V	1, 2, 3	$0.3V_{DD2}$		
		A Port = 5.0 V	All	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	1, 2, 3	$0.3V_{DD2}$		
		B Port = 3.3 V	01	V_{DD1} = 3.13 V and 3.6 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3	$0.3V_{DD1}$		
		B Port = 3.3 V	02, 03, 04, 05, 06, 07	V_{DD1} = 3.0 V and 3.6 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3	$0.3V_{DD1}$		
		B Port = 3.3 V	08	V_{DD1} = 2.7 V and 3.6 V, V_{DD2} = 2.7 V and 3.6 V	1, 2, 3	$0.3V_{DD1}$		
		B Port = 5.0 V	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3	$0.3V_{DD1}$		
		B Port = 5.0 V	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3	$0.3V_{DD1}$		
		B Port = 5.0 V	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 2.7 V and 3.6 V	1, 2, 3	$0.3V_{DD1}$		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ 3/ -55°C ≤ T_C ≤ +125°C For 5.0 V supply: +4.5 V ≤ V_{DD1} ≤ +5.5 V For 3.3 V supply: +3.0 V ≤ V_{DD2} ≤ +3.6 V unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/		Unit
						Min	Max	
Schmitt trigger range of	V_H 6/	A Port = 3.3 V	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3	0.4		V
		A Port = 3.3 V	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3	0.4		
		A Port = 3.3 V	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 2.7 V and 3.6 V	1, 2, 3	0.4		
		A Port = 5.0 V	All	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	1, 2, 3	0.6		
		B Port = 3.3 V	01	V_{DD1} = 3.13 V and 3.6 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3	0.4		
		B Port = 3.3 V	02, 03, 04, 05, 06, 07	V_{DD1} = 3.0 V and 3.6 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3	0.4		
		B Port = 3.3 V	08	V_{DD1} = 2.7 V and 3.6 V, V_{DD2} = 2.7 V and 3.6 V	1, 2, 3	0.4		
		B Port = 5.0 V	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3	0.6		
		B Port = 5.0 V	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3	0.6		
		B Port = 5.0 V	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 2.7 V and 3.6 V	1, 2, 3	0.6		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ 3/ -55°C ≤ T_C ≤ +125°C For 5.0 V supply: +4.5 V ≤ V_{DD1} ≤ +5.5 V For 3.3 V supply: +3.0 V ≤ V_{DD2} ≤ +3.6 V unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/		Unit
						Min	Max	
Input current high	I_{IH} 7/	A Port = 3.3 V For input under test, $V_{IN} = V_{DD2}$ Other inputs, $V_{IN} = V_{DD2}$ or V_{SS}	All	V_{DD1} = 5.5 V, V_{DD2} = 3.6 V	1, 2, 3		3.0	μA
		A Port = 5.0 V For input under test, $V_{IN} = V_{DD2}$ Other inputs, $V_{IN} = V_{DD2}$ or V_{SS}	All	V_{DD1} = 5.5 V, V_{DD2} = 5.5 V	1, 2, 3		3.0	
		B Port = 3.3 V For input under test, $V_{IN} = V_{DD1}$ Other inputs, $V_{IN} = V_{DD1}$ or V_{SS}	All	V_{DD1} = 3.6 V, V_{DD2} = 3.6 V	1, 2, 3		3.0	
		B Port = 5.0 V For input under test, $V_{IN} = V_{DD1}$ Other inputs, $V_{IN} = V_{DD1}$ or V_{SS}	All	V_{DD1} = 5.5 V, V_{DD2} = 3.6 V	1, 2, 3		3.0	
Input current low	I_{IL} 7/	A Port = 3.3 V For input under test, $V_{IN} = V_{SS}$ Other inputs, $V_{IN} = V_{DD2}$ or V_{SS}	All	V_{DD1} = 5.5 V, V_{DD2} =3.6 V	1, 2, 3	-1.0		μA
		A Port = 5.0 V For input under test, $V_{IN} = V_{SS}$ Other inputs, $V_{IN} = V_{DD1}$ or V_{SS}	All	V_{DD1} = 5.5 V, V_{DD2} = 5.5 V	1, 2, 3	-1.0		
		B Port = 3.3 V For input under test, $V_{IN} = V_{SS}$ Other inputs, $V_{IN} = V_{DD1}$ or V_{SS}	All	V_{DD1} = 3.6 V, V_{DD2} = 3.6 V	1, 2, 3	-1.0		
		B Port = 5.0 V For input under test, $V_{IN} = V_{SS}$ Other inputs, $V_{IN} = V_{DD1}$ or V_{SS}	All	V_{DD1} = 5.5 V, V_{DD2} = 3.6 V	1, 2, 3	-1.0		
Input current cold spare mode	I_{CS} 8/	A Port = B Port = 5.5 V = V_{IN} DIRx = 5.5 V, $\overline{OEx}$ = 5.5 V	All	V_{DD1} = 0.0 V, V_{DD2} = 0.0 V	1, 2, 3	-1.0	5.0	μA
		A Port = B Port = 5.5 V = V_{IN} DIRx = 0.0 V, $\overline{OEx}$ = 5.5 V	All	V_{DD1} = 0.0 V, V_{DD2} = 0.0 V	1, 2, 3	-1.0	5.0	
		A Port = B Port = 5.5 V = V_{IN} DIRx = 5.5 V, $\overline{OEx}$ = 0.0 V	All	V_{DD1} = 0.0 V, V_{DD2} = 0.0 V	1, 2, 3	-1.0	5.0	
		A Port = B Port = 5.5 V = V_{IN} DIRx = 0.0 V, $\overline{OEx}$ = 0.0	All	V_{DD1} = 0.0 V, V_{DD2} = 0.0 V	1, 2, 3	-1.0	5.0	
Input current warm spare mode	I_{WSA} 8/	A Port = B Port = 5.5 V = V_{IN}	06, 07	V_{DD1} = 0.0 V, V_{DD2} = 3.6 V	1, 2, 3	-1.0	5.0	μA
		A Port = B Port = 5.5 V = V_{IN}	06, 07	V_{DD1} = 0.0 V, V_{DD2} = 5.5 V	1, 2, 3	-1.0	5.0	
	I_{WSA} 8/	A Port = B Port = 5.5 V = V_{IN}	06, 07	V_{DD1} = 3.6 V, V_{DD2} = 0.0 V	1, 2, 3	-1.0	5.0	
		A Port = B Port = 5.5 V = V_{IN}	06, 07	V_{DD1} = 5.5 V, V_{DD2} = 0.0 V	1, 2, 3	-1.0	5.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ 3/ $-55°C \leq T_C \leq +125°C$ For 5.0 V supply: $+4.5 V \leq V_{DD1} \leq +5.5 V$ For 3.3 V supply: $+3.0 V \leq V_{DD2} \leq +3.6 V$ unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/		Unit
						Min	Max	
Low level output voltage	V_{OL1} 9/	A Port = 3.3 V, I_{OL} = +8 mA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	01	V_{DD1} = 4.5 V, V_{DD2} = 3.13 V	1, 2, 3		0.5	V
		A Port = 3.3 V, I_{OL} = +8 mA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V, V_{DD2} = 3.0 V	1, 2, 3		0.5	
		A Port = 3.3 V, I_{OL} = +8 mA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	08	V_{DD1} = 4.5 V, V_{DD2} = 2.7 V	1, 2, 3		0.5	
		A Port = 5.0 V, I_{OL} = +8 mA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	All	V_{DD1} = 4.5 V, V_{DD2} = 4.5 V	1, 2, 3		0.4	
		B Port = 3.3 V, I_{OL} = +8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	01	V_{DD1} = 3.13 V, V_{DD2} = 3.13 V	1, 2, 3		0.5	
		B Port = 3.3 V, I_{OL} = +8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	02, 03, 04, 05, 06, 07	V_{DD1} = 3.0 V, V_{DD2} = 3.0 V	1, 2, 3		0.5	
		B Port = 3.3 V, I_{OL} = +8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	08	V_{DD1} = 2.7 V, V_{DD2} = 2.7 V	1, 2, 3		0.5	
		B Port = 5.0 V, I_{OL} = +8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	01	V_{DD1} = 4.5 V, V_{DD2} = 3.13 V	1, 2, 3		0.4	
		B Port = 5.0 V, I_{OL} = +8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V, V_{DD2} = 3.0 V	1, 2, 3		0.4	
		B Port = 5.0 V, I_{OL} = +8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	08	V_{DD1} = 4.5 V, V_{DD2} = 2.7 V	1, 2, 3		0.4	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ 3/ $-55°C \leq T_C \leq +125°C$ For 5.0 V supply: $+4.5\ V \leq V_{DD1} \leq +5.5\ V$ For 3.3 V supply: $+3.0\ V \leq V_{DD2} \leq +3.6\ V$ unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/		Unit
						Min	Max	
Low level output voltage	V_{OL2} 10/	A Port = 3.3 V, I_{OL} = +100 µA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	01	V_{DD1} = 4.5 V, V_{DD2} = 3.13 V	1, 2, 3		0.2	V
		A Port = 3.3 V, I_{OL} = +100 µA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V, V_{DD2} = 3.0 V	1, 2, 3		0.2	
		A Port = 3.3 V, I_{OL} = +100 µA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	08	V_{DD1} = 4.5 V, V_{DD2} = 2.7 V	1, 2, 3		0.2	
		A Port = 5.0 V, I_{OL} = +100 µA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	All	V_{DD1} = 4.5 V, V_{DD2} = 4.5 V	1, 2, 3		0.2	
		B Port = 3.3 V, I_{OL} = +100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	01	V_{DD1} = 3.13 V, V_{DD2} = 3.13 V	1, 2, 3		0.2	
		B Port = 3.3 V, I_{OL} = +100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	02, 03, 04, 05, 06, 07	V_{DD1} = 3.0 V, V_{DD2} = 3.0 V	1, 2, 3		0.2	
		B Port = 3.3 V, I_{OL} = +100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	08	V_{DD1} = 2.7 V, V_{DD2} = 2.7 V	1, 2, 3		0.2	
		B Port = 5.0 V, I_{OL} = +100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	01	V_{DD1} = 4.5 V, V_{DD2} = 3.13 V	1, 2, 3		0.2	
		B Port = 5.0 V, I_{OL} = +100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V, V_{DD2} = 3.0 V	1, 2, 3		0.2	
		B Port = 5.0 V, I_{OL} = +100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	08	V_{DD1} = 4.5 V, V_{DD2} = 2.7 V	1, 2, 3		0.2	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ 3/ -55°C ≤ T_C ≤ +125°C For 5.0 V supply: +4.5 V ≤ V_{DD1} ≤ +5.5 V For 3.3 V supply: +3.0 V ≤ V_{DD2} ≤ +3.6 V unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/ Min	Limits 5/ Max	Unit
High level output voltage	V_{OH1} 9/	A Port = 3.3 V, I_{OH} = -8 mA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	01	V_{DD1} = 4.5 V, V_{DD2} = 3.13 V	1, 2, 3	V_{DD2} – 0.9 V		V
		A Port = 3.3 V, I_{OH} = -8 mA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V, V_{DD2} = 3.0 V	1, 2, 3	V_{DD2} – 0.9 V		
		A Port = 3.3 V, I_{OH} = -8 mA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	08	V_{DD1} = 4.5 V, V_{DD2} = 2.7 V	1, 2, 3	V_{DD2} – 0.9 V		
		A Port = 5.0 V, I_{OH} = -8 mA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	All	V_{DD1} = 4.5 V, V_{DD2} = 4.5 V	1, 2, 3	V_{DD2} – 0.7 V		
		B Port = 3.3 V, I_{OH} = -8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	01	V_{DD1} = 3.13 V, V_{DD2} = 3.13 V	1, 2, 3	V_{DD1} – 0.9 V		
		B Port = 3.3 V, I_{OH} = -8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	02, 03, 04, 05, 06, 07	V_{DD1} = 3.0 V, V_{DD2} = 3.0 V	1, 2, 3	V_{DD1} – 0.9 V		
		B Port = 3.3 V, I_{OH} = -8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	08	V_{DD1} = 2.7 V, V_{DD2} = 2.7 V	1, 2, 3	V_{DD1} – 0.9 V		
		B Port = 5.0 V, I_{OH} = -8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	01	V_{DD1} = 4.5 V, V_{DD2} = 3.13 V	1, 2, 3	V_{DD1} – 0.7 V		
		B Port = 5.0 V, I_{OH} = -8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V, V_{DD2} = 3.0 V	1, 2, 3	V_{DD1} – 0.7 V		
		B Port = 5.0 V, I_{OH} = -8 mA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	08	V_{DD1} = 4.5 V, V_{DD2} = 2.7 V	1, 2, 3	V_{DD1} – 0.7 V		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ 3/ $-55°C \leq T_C \leq +125°C$ For 5.0 V supply: $+4.5 V \leq V_{DD1} \leq +5.5 V$ For 3.3 V supply: $+3.0 V \leq V_{DD2} \leq +3.6 V$ unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/		Unit
						Min	Max	
High level output voltage	V_{OH2} 10/	A Port = 3.3 V, I_{OH} = -100 µA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	01	V_{DD1} = 4.5 V, V_{DD2} = 3.13 V	1, 2, 3	V_{DD2} - 0.2 V		V
		A Port = 3.3 V, I_{OH} = -100 µA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V, V_{DD2} = 3.0 V	1, 2, 3	V_{DD2} - 0.2 V		
		A Port = 3.3 V, I_{OH} = -100 µA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	08	V_{DD1} = 4.5 V, V_{DD2} = 2.7 V	1, 2, 3	V_{DD2} - 0.2 V		
		A Port = 5.0 V, I_{OH} = -100 µA For all inputs affecting output under test, $V_{IN} = V_{DD2}$ or V_{SS}	All	V_{DD1} = 4.5 V, V_{DD2} = 4.5 V	1, 2, 3	V_{DD2} - 0.2 V		
		B Port = 3.3 V, I_{OH} = -100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	01	V_{DD1} = 3.13 V, V_{DD2} = 3.13 V	1, 2, 3	V_{DD1} - 0.2 V		
		B Port = 3.3 V, I_{OH} = -100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	02, 03, 04, 05, 06, 07	V_{DD1} = 3.0 V, V_{DD2} = 3.0 V	1, 2, 3	V_{DD1} - 0.2 V		
		B Port = 3.3 V, I_{OH} = -100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	08	V_{DD1} = 2.7 V, V_{DD2} = 2.7 V	1, 2, 3	V_{DD1} - 0.2 V		
		B Port = 5.0 V, I_{OH} = -100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	01	V_{DD1} = 4.5 V, V_{DD2} = 3.13 V	1, 2, 3	V_{DD1} - 0.2 V		
		B Port = 5.0 V, I_{OH} = -100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V, V_{DD2} = 3.0 V	1, 2, 3	V_{DD1} - 0.2 V		
		B Port = 5.0 V, I_{OH} = -100 µA For all inputs affecting output under test, $V_{IN} = V_{DD1}$ or V_{SS}	08	V_{DD1} = 4.5 V, V_{DD2} = 2.7 V	1, 2, 3	V_{DD1} - 0.2 V		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ 3/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/ Min	Limits 5/ Max	Unit
Output current (Sink)	I_{OL} 11/	A Port = 3.3 V $V_{IN} = V_{SS}$ $V_{OL} = 0.5\ V$	01	$V_{DD1} = 4.5\ V$, $V_{DD2} = 3.13\ V$	1, 2, 3	8.0		mA
			02, 03, 04, 05, 06, 07	$V_{DD1} = 4.5\ V$, $V_{DD2} = 3.0\ V$	1, 2, 3	8.0		
			08	$V_{DD1} = 4.5\ V$, $V_{DD2} = 2.7\ V$	1, 2, 3	8.0		
		A Port = 5.0 V $V_{IN} = V_{SS;}\ V_{OL} = 0.4\ V$	All	$V_{DD1} = 4.5\ V$, $V_{DD2} = 4.5\ V$	1, 2, 3	8.0		
		B Port = 3.3 V $V_{IN} = V_{SS;}$ $V_{OL} = 0.5\ V$	01	$V_{DD1} = 3.13\ V$, $V_{DD2} = 3.13\ V$	1, 2, 3	8.0		
			02, 03, 04, 05, 06, 07	$V_{DD1} = 3.0\ V$, $V_{DD2} = 3.0\ V$	1, 2, 3	8.0		
			08	$V_{DD1} = 2.7\ V$, $V_{DD2} = 2.7\ V$	1, 2, 3	8.0		
		B Port = 5.0 V $V_{IN} = V_{SS}$ $V_{OL} = 0.4\ V$	01	$V_{DD1} = 4.5\ V$, $V_{DD2} = 3.13\ V$	1, 2, 3	8.0		
			02, 03, 04, 05, 06, 07	$V_{DD1} = 4.5\ V$, $V_{DD2} = 3.0\ V$	1, 2, 3	8.0		
			08	$V_{DD1} = 4.5\ V$, $V_{DD2} = 2.7\ V$	1, 2, 3	8.0		
Output current (source)	I_{OH} 11/	A Port = 3.3 V $V_{IN} = V_{DD2}$ or V_{SS} $V_{OH} = V_{DD2} - 0.9\ V$	01	$V_{DD1} = 4.5\ V$, $V_{DD2} = 3.13\ V$	1, 2, 3	-8.0		mA
			02, 03, 04, 05, 06, 07	$V_{DD1} = 4.5\ V$, $V_{DD2} = 3.0\ V$	1, 2, 3	-8.0		
			08	$V_{DD1} = 4.5\ V$, $V_{DD2} = 2.7\ V$	1, 2, 3	-8.0		
		A Port = 5.0 V $V_{IN} = V_{DD2}$ or V_{SS} $V_{OH} = V_{DD2} - 0.7\ V$	All	$V_{DD1} = 4.5\ V$, $V_{DD2} = 4.5\ V$	1, 2, 3	-8.0		
		B Port = 3.3 V $V_{IN} = V_{DD1}$ or V_{SS} $V_{OH} = V_{DD1} - 0.9\ V$	01	$V_{DD1} = 3.13\ V$, $V_{DD2} = 3.13\ V$	1, 2, 3	-8.0		
			02, 03, 04, 05, 06, 07	$V_{DD1} = 3.0\ V$, $V_{DD2} = 3.0\ V$	1, 2, 3	-8.0		
			08	$V_{DD1} = 2.7\ V$, $V_{DD2} = 2.7\ V$	1, 2, 3	-8.0		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ 3/ $-55°C \leq T_C \leq +125°C$ For 5.0 V supply: $+4.5\ V \leq V_{DD1} \leq +5.5\ V$ For 3.3 V supply: $+3.0\ V \leq V_{DD2} \leq +3.6\ V$ unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/		Unit
						Min	Max	
Output current (Source)	I_{OH} 11/	B Port = 5.0 V $V_{IN} = V_{DD1}$ or V_{SS} $V_{OH} = V_{DD1} - 0.7\ V$	01	$V_{DD1} = 4.5\ V$, $V_{DD2} = 3.13\ V$	1, 2, 3	-8.0		
		B Port = 5.0 V $V_{IN} = V_{DD1}$ or V_{SS} $V_{OH} = V_{DD1} - 0.7\ V$	02, 03, 04, 05, 06, 07	$V_{DD1} = 4.5\ V$, $V_{DD2} = 3.0\ V$	1, 2, 3	-8.0		
		B Port = 5.0 V $V_{IN} = V_{DD2}$ or $V_{SS,}$ $V_{OH} = V_{DD1} - 0.7\ V$	08	$V_{DD1} = 4.5\ V$, $V_{DD2} = 2.7\ V$	1, 2, 3	-8.0		
Three-state output leakage current high	I_{OZH} 7/	A Port = 3.3 V For input under test, $V_{IN} = V_{DD2}$ Other inputs, $V_{IN} = V_{DD2}$ or V_{SS} $V_{OUT} = V_{DD2}$	All	$V_{DD1} = 5.5\ V$, $V_{DD2} = 3.6\ V$	1, 2, 3		3.0	µA
		A Port = 5.0 V For input under test, $V_{IN} = V_{DD2}$ Other inputs, $V_{IN} = V_{DD2}$ or V_{SS} $V_{OUT} = V_{DD2}$	All	$V_{DD1} = 5.5\ V$, $V_{DD2} = 5.5\ V$	1, 2, 3		3.0	
		B Port = 3.3 V For input under test, $V_{IN} = V_{DD1}$ Other inputs, $V_{IN} = V_{DD1}$ or V_{SS} $V_{OUT} = V_{DD1}$	All	$V_{DD1} = 3.6\ V$, $V_{DD2} = 3.6\ V$	1, 2, 3		3.0	
		B Port = 5.0 V For input under test, $V_{IN} = V_{DD1}$ Other inputs, $V_{IN} = V_{DD1}$ or V_{SS} $V_{OUT} = V_{DD1}$	All	$V_{DD1} = 5.5\ V$, $V_{DD2} = 3.6\ V$	1, 2, 3		3.0	
Three-state output leakage current low	I_{OZL} 7/	A Port = 3.3 V For input under test, $V_{IN} = V_{SS}$ Other inputs, $V_{IN} = V_{DD2}$ or V_{SS} $V_{OUT} = V_{SS}$	All	$V_{DD1} = 5.5\ V$, $V_{DD2} = 3.6\ V$	1, 2, 3	-1.0		µA
		A Port = 5.0 V For input under test, $V_{IN} = V_{SS}$ Other inputs, $V_{IN} = V_{DD2}$ or V_{SS} $V_{OUT} = V_{SS}$	All	$V_{DD1} = 5.5\ V$, $V_{DD2} = 5.5\ V$	1, 2, 3	-1.0		
		B Port = 3.3 V For input under test, $V_{IN} = V_{SS}$ Other inputs, $V_{IN} = V_{DD1}$ or V_{SS} $V_{OUT} = V_{SS}$	All	$V_{DD1} = 3.6\ V$, $V_{DD2} = 3.6\ V$	1, 2, 3	-1.0		
		B Port = 5.0 V For input under test, $V_{IN} = V_{SS}$ Other inputs, $V_{IN} = V_{DD1}$ or V_{SS} $V_{OUT} = V_{SS}$	All	$V_{DD1} = 5.5\ V$, $V_{DD2} = 3.6\ V$	1, 2, 3	-1.0		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ 3/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5 V \le V_{DD1} \le +5.5 V$ For 3.3 V supply: $+3.0 V \le V_{DD2} \le +3.6 V$ unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/		Unit
						Min	Max	
Short circuit output current	I_{OS} 12/ 13/	A Port = 3.3 V $V_{OUT} = V_{DD2}$ or V_{SS}	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3	-100.0	100.0	mA
		A Port = 3.3 V $V_{OUT} = V_{DD2}$ or V_{SS}	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3	-100.0	100.0	
		A Port = 3.3 V $V_{OUT} = V_{DD2}$ or V_{SS}	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 2.7 V and 3.6 V	1, 2, 3	-100.0	100.0	
		A Port = 5.0 V $V_{OUT} = V_{DD2}$ or V_{SS}	All	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	1, 2, 3	-200.0	200.0	
		B Port = 3.3 V $V_{OUT} = V_{DD1}$ or V_{SS}	01	V_{DD1} = 3.13 V and 3.6 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3	-100.0	100.0	
		B Port = 3.3 V $V_{OUT} = V_{DD1}$ or V_{SS}	02, 03, 04, 05, 06, 07	V_{DD1} = 3.0 V and 3.6 V, V_{DD2} = 3.0V and 3.6 V	1, 2, 3	-100.0	100.0	
		B Port = 3.3 V $V_{OUT} = V_{DD1}$ or V_{SS}	08	V_{DD1} = 2.7 V and 3.6 V, V_{DD2} = 2.7V and 3.6 V	1, 2, 3	-100.0	100.0	
		B Port = 5.0 V $V_{OUT} = V_{DD1}$ or V_{SS}	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	1, 2, 3	-200.0	200.0	
		B Port = 5.0 V $V_{OUT} = V_{DD1}$ or V_{SS}	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	1, 2, 3	-200.0	200.0	
		B Port = 5.0 V $V_{OUT} = V_{DD1}$ or V_{SS}	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 2.7 V and 3.6 V	1, 2, 3	-200.0	200.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ 3/ -55°C ≤ T_C ≤ +125°C For 5.0 V supply: +4.5 V ≤ V_{DD1} ≤ +5.5 V For 3.3 V supply: +3.0 V ≤ V_{DD2} ≤ +3.6 V unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/		Unit
						Min	Max	
Power dissipation	P_D 12/ 14/ 15/	A Port = 3.3 V C_L = 40 pF per switching output	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3 13 V and 3.6 V	4, 5, 6		1.5	mW/ MHz
		A Port = 3.3 V C_L = 40 pF per switching output	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	4, 5, 6		1.5	
		A Port = 3.3 V C_L = 50 pF per switching output	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 2.7 V and 3.6 V	4, 5, 6		1.5	
		A Port = 5.0 V C_L = 40 pF per switching output	01 to 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	4, 5, 6		2.0	
		A Port = 5.0 V C_L = 50 pF per switching output	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	4, 5, 6		2.0	
		B Port = 3.3 V C_L = 40 pF per switching output	01	V_{DD1} = 3.13 V and 3.6 V, V_{DD2} = 3.13 V and 3.6 V	4, 5, 6		1.5	
		B Port = 3.3 V C_L = 40 pF per switching output	02, 03, 04, 05, 06, 07	V_{DD1} = 3.0 V and 3.6 V, V_{DD2} = 3.0 V and 3.6 V	4, 5, 6		1.5	
		B Port = 3.3 V C_L = 50 pF per switching output	08	V_{DD1} = 2.7 V and 3.6 V, V_{DD2} = 2.7 V and 3.6 V	4, 5, 6		1.5	
		B Port = 5.0 V C_L = 40 pF per switching output	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	4, 5, 6		2.0	
		B Port = 5.0 V C_L = 40 pF per switching output	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	4, 5, 6		2.0	
		B Port = 5.0 V C_L = 50 pF per switching output	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 2.7 V and 3.6 V	4, 5, 6		2.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ 3/ $-55°C \leq T_C \leq +125°C$ For 5.0 V supply: $+4.5 V \leq V_{DD1} \leq +5.5 V$ For 3.3 V supply: $+3.0 V \leq V_{DD2} \leq +3.6 V$ unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/ Min	Limits 5/ Max	Unit
Quiescent supply current	I_{DDQ}	A Port = 5.0 V $V_{IN} = V_{DD2}$ or V_{SS}	01, 02, 03, 04, 05, 08	V_{DD1} = 5.5 V, V_{DD2} = 5.5 V	1		10.0	µA
					2, 3		100.0	
		A Port = 5.0 V, $V_{IN} = V_{DD2}$ or V_{SS} M, D, P, L, R 3/			1		500.0	
		B Port = 5.0 V $V_{IN} = V_{DD1}$ or V_{SS}	01, 02, 03, 04, 05, 08	V_{DD1} = 5.5 V, V_{DD2} = 5.5 V	1		10.0	µA
					2, 3		100.0	
		B Port = 5.0 V, $V_{IN} = V_{DD1}$ or V_{SS} M, D, P, L, R 3/			1		500.0	
		A Port = 5.0 V $V_{IN} = V_{DD2}$ or V_{SS}	06, 07	V_{DD1} = 5.5 V, V_{DD2} = 5.5 V	1		60	µA
					2, 3		100	
		A Port = 5.0 V, $V_{IN} = V_{DD2}$ or V_{SS} M, D, P, L, R 3/			1		100	
		B Port = 5.0 V $V_{IN} = V_{DD1}$ or V_{SS}	06, 07	V_{DD1} = 5.5 V, V_{DD2} = 5.5 V	1		60	µA
					2, 3		100	
		B Port = 5.0 V$V_{IN} = V_{DD1}$ or V_{SS} M, D, P, L, R 3/			1		100	
Input capacitance	C_{IN}	f = 1 MHz, See 4.4.1c	All	V_{DD1}, V_{DD2} = 0.0 V	4		15	pF
Output capacitance	C_{OUT}	f = 1 MHz, See 4.4.1c	All	V_{DD1}, V_{DD2} = 0.0 V	4		15	pF

See footnotes at end of table

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ 3/ $-55°C \le T_C \le +125°C$ For 5.0 V supply: $+4.5\ V \le V_{DD1} \le +5.5\ V$ For 3.3 V supply: $+3.0\ V \le V_{DD2} \le +3.6\ V$ unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/ Min	Limits 5/ Max	Unit
Functional test	16/	$V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$ See 4.4.1b	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	7, 8	L	H	
		M, D, P, L, R 3/	01		7	L	H	
		$V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$ See 4.4.1b	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	7, 8	L	H	
		M, D, P, L, R 3/	02, 03, 04, 05, 06, 07		7	L	H	
		$V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$ See 4.4.1b	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 2.7 V and 3.6 V	7, 8	L	H	
Propagation delay time, data to bus (active low and active high)	t_{PLH} and t_{PHL} 17/	B Port = 5 V, A Port = 3.3 V C_L = 40 pF, see figure 5	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	9, 10, 11	1.0	20.0	ns
		B Port = 5 V, A Port = 3.3 V C_L = 40 pF, see figure 5	02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	9, 10, 11	1.0	20.0	
			04, 05, 06, 07			3.5	11.0	
		B Port = 5 V, A Port = 3.3 V C_L = 50 pF, see figure 5	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 2.7 V and 3.6 V	9, 10, 11	1.0	20.0	
		A Port = B Port = 5 V operation C_L = 40 pF, see figure 5	01, 02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	15.0	
			04, 05, 06, 07			3.5	9.0	
		A Port = B Port = 5 V operation C_L = 50 pF, see figure 5	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	15.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ 3/ -55°C ≤ T_C ≤ +125°C For 5.0 V supply: +4.5 V ≤ V_{DD1} ≤ +5.5 V For 3.3 V supply: +3.0 V ≤ V_{DD2} ≤ +3.6 V unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/ Min	Limits 5/ Max	Unit
Propagation delay time, data to bus active low and active high)	t_{PLH} and t_{PHL} 17/	A Port = B Port = 3.3 V C_L = 40 pF, see figure 5	01	V_{DD1} = 3.13 V and 3.6 V, V_{DD2} = 3.13 V and 3.6 V	9, 10, 11	1.0	20.0	ns
		A Port = B Port = 3.3 V C_L = 40 pF, see figure 5	02, 03	V_{DD1} = 3.0 V and 3.6 V, V_{DD2} = 3.0 V and 3.6 V	9, 10, 11	1.0	20.0	
			04, 05, 06, 07			3.5	11.0	
		A Port = B Port = 3.3 V C_L = 50 pF, see figure 5	08	V_{DD1} = 2.7 V and 3.6 V, V_{DD2} = 2.7 V and 3.6 V	9, 10, 11	1.0	20.	
Propagation delay time, output enable, $\overline{OEx}$ to bus (active low and active high)	t_{PZL1} and t_{PZH1} 17/	A Port = 3.3 V, B Port = 5 V C_L = 40 pF, see figure 5	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.13V and 3.6 V	9, 10, 11	1.0	18.0	ns
			02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0V and 3.6 V		1.0	18.0	
			04, 05, 06, 07			2.5	16.0	
		A Port = 3.3 V, B Port = 5.0 V C_L = 50 pF, see figure 5	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 2.7 V and 3.6 V	9, 10, 11	1.0	18.0	
		A Port = B Port = 5.0 V operation C_L = 40 pF, see figure 5	01, 02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	12.0	
			04, 05, 06, 07			3.0	9.0	
		A Port = B Port = 5.0 V C_L = 50 pF, see figure 5	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	12.0	
		A Port = B Port = 3.3 V operation C_L = 40 pF, see figure 5	01	V_{DD1} = 3.13 V and 3.6 V, V_{DD2} = 3.13 V and 3.6 V	9, 10, 11	1.0	18.0	
			02, 03	V_{DD1} = 3.0 V and 3.6 V, V_{DD2} = 3.0 V and 3.6 V	9, 10, 11	1.0	18.0	
			04, 05, 06, 07			2.5	16.0	
		A Port = B Port = 3.3 C_L = 50 pF, see figure 5	08	V_{DD1} = 2.7 V and 3.6 V, V_{DD2} = 2.7 V and 3.6 V	9, 10, 11	1.0	18.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ 3/ $-55°C \leq T_C \leq +125°C$ For 5.0 V supply: $+4.5\ V \leq V_{DD1} \leq +5.5\ V$ For 3.3 V supply: $+3.0\ V \leq V_{DD2} \leq +3.6\ V$ unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/ Min	Limits 5/ Max	Unit
Propagation delay time, output disable, $\overline{OEx}$ to bus (high impedance)	t_{PLZ1} and t_{PHZ1} 17/	B Port = 5 V, A Port = 3.3 V C_L = 40 pF, see figure 5	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	9, 10, 11	1.0	20.0	ns
		B Port = 5 V, A Port = 3.3 V C_L = 40 pF, see figure 5	02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	9, 10, 11	1.0	20.0	
			04, 05, 06, 07			2.5	16.0	
		B Port = 5.0 V, A Port = 3.3 V C_L = 50 pF, see figure 5	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 2.7 V and 3.6 V	9, 10, 11	1.0	20.0	
		A Port = B Port = 5 V operation C_L = 40 pF, see figure 5	01, 02, 03	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	15.0	
			04, 05, 06, 07			3.0	9.0	
		A Port = B Port = 5.0 V C_L = 50 pF, see figure 5	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	15.0	
		A Port = B Port = 3.3 V operation C_L = 40 pF, see figure 5	01	V_{DD1} = 3.13 V and 3.6 V, V_{DD2} = 3.13 V and 3.6 V	9, 10, 11	1.0	20.0	
		A Port = B Port = 3.3 V operation C_L = 40 pF, see figure 5	02, 03	V_{DD1} = 3.0 V and 3.6 V, V_{DD2} = 3.0 V and 3.6 V	9, 10, 11	1.0	20.0	
			04, 05, 06, 07			2.5	16.0	
		A Port = B Port = 3.3 C_L = 50 pF, see figure 5	08	V_{DD1} = 2.7 V and 3.6 V, V_{DD2} = 2.7 V and 3.6 V	9, 10, 11	1.0	20.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ 3/ -55°C ≤ T_C ≤ +125°C For 5.0 V supply: +4.5 V ≤ V_{DD1} ≤ +5.5 V For 3.3 V supply: +3.0 V ≤ V_{DD2} ≤ +3.6 V unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/		Unit
						Min	Max	
Propagation delay time, output enable, DIRx to bus (active low and active high)	t_{PZL2}, t_{PZH2} 18/	B Port = 5 V, A Port = 3.3 V C_L = 40 pF, see figure 5	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	9, 10, 11	1.0	18.0	ns
		B Port = 5 V, A Port = 3.3 V C_L = 40 pF, see figure 5	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	9, 10, 11	1.0	18.0	
		B Port = 5.0 V, A Port = 3.3 V C_L = 50 pF, see figure 5	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 2.7 V and 3.6 V	9, 10, 11	1.0	18.0	
		A Port = B Port = 5 V operation C_L = 40 pF, see figure 5	01 to 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	12.0	
		A Port = B Port = 5.0 V C_L = 50 pF, see figure 5	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	12.0	
		A Port = B Port = 3.3 V operation C_L = 40 pF, see figure 5	01	V_{DD1} = 3.13 V and 3.6 V, V_{DD2} = 3.13 V and 3.6 V	9, 10, 11	1.0	18.0	
		A Port = B Port = 3.3 V operation C_L = 40 pF, see figure 5	02, 03, 04, 05, 06, 07	V_{DD1} = 3.0 V and 3.6 V, V_{DD2} = 3.0 V and 3.6 V	9, 10, 11	1.0	18.0	
		A Port = B Port = 3.3 C_L = 50 pF, see figure 5	08	V_{DD1} = 2.7 V and 3.6 V, V_{DD2} = 2.7 V and 3.6 V	9, 10, 11	1.0	18.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ 3 $-55°C \leq T_C \leq +125°C$ For 5.0 V supply: $+4.5\ V \leq V_{DD1} \leq +5.5\ V$ For 3.3 V supply: $+3.0\ V \leq V_{DD2} \leq +3.6\ V$ unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/		Unit
						Min	Max	
Propagation delay time, output disable, DIRx to bus (high impedance)	t_{PLZ2}, t_{PHZ2} 18/	B Port = 5 V, A Port = 3.3 V C_L = 40 pF, see figure 5	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	9, 10, 11	1.0	20.0	ns
		B Port = 5 V, A Port = 3.3 V C_L = 40 pF, see figure 5	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	9, 10, 11	1.0	20.0	
		B Port = 5 V, A Port = 3.3 V C_L = 50 pF, see figure 5	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 2.7 V and 3.6 V	9, 10, 11	1.0	20.0	
		A Port = B Port = 5 V operation C_L = 40 pF, see figure 5	01 to 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	15.0	
		A Port = B Port = 5.0 V C_L = 50 pF, see figure 5	08	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11	1.0	15.0	
		A Port = B Port = 3.3 V operation C_L = 40 pF, see figure 5	01	V_{DD1} = 3.13 V and 3.6 V, V_{DD2} = 3.13 V and 3.6 V	9, 10, 11	1.0	20.0	
		A Port = B Port, 3.3 V operation C_L = 40 pF, see figure 5	02, 03, 04, 05, 06, 07	V_{DD1} = 3.0 V and 3.6 V, V_{DD2} = 3.0 V and 3.6 V	9, 10, 11	1.0	20.0	
		A Port = B Port = 3.3 C_L = 50 pF, see figure 5	08	V_{DD1} = 2.7 V and 3.6 V, V_{DD2} = 2.7 V and 3.6 V	9, 10, 11	1.0	20.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ 3/ -55°C ≤ T_C ≤ +125°C For 5.0 V supply: +4.5 V ≤ V_{DD1} ≤ +5.5 V For 3.3 V supply: +3.0 V ≤ V_{DD2} ≤ +3.6 V unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/ Min	Limits 5/ Max	Unit
Skew between outputs.	t_{SKEW} 19/ 21/	B Port = 5 V, A Port = 3.3 V C_L = 40 pF	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	9, 10, 11		600	ps
		B Port = 5 V, A Port = 3.3 V C_L = 40 pF	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	9, 10, 11		600	
		A Port = B Port, 5 V operation C_L = 40 pF	01 to 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11		600	
		A Port = B Port, 3.3 V operation C_L = 40 pF	01	V_{DD1} = 3.13 V and 3.6 V, V_{DD2} = 3.13 V and 3.6 V	9, 10, 11		600	
		A Port = B Port, 3.3 V operation C_L = 40 pF	02, 03, 04, 05, 06, 07	V_{DD1} = 3.0 V and 3.6 V, V_{DD2} = 3.0 V and 3.6 V	9, 10, 11		600	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ 2/ 3/ -55°C ≤ T_C ≤ +125°C For 5.0 V supply: +4.5 V ≤ V_{DD1} ≤ +5.5 V For 3.3 V supply: +3.0 V ≤ V_{DD2} ≤ +3.6 V unless otherwise specified	Device type	V_{DD} 4/	Group A subgroups	Limits 5/		Unit
						Min	Max	
Differential skew between outputs	t_{DSKEW} 20/ 22/	B Port = 5 V, A Port = 3.3 V C_L = 40 pF	01	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.13 V and 3.6 V	9, 10, 11		1.5	ns
		B Port = 5 V, A Port = 3.3 V C_L = 40 pF	02, 03, 04, 05, 06, 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 3.0 V and 3.6 V	9, 10, 11		1.5	
		A Port = B Port, 5 V operation C_L = 40 pF	01 to 07	V_{DD1} = 4.5 V and 5.5 V, V_{DD2} = 4.5 V and 5.5 V	9, 10, 11		1.5	
		A Port = B Port, 3.3 V operation C_L = 40 pF	01	V_{DD1} = 3.13 V and 3.6 V, V_{DD2} = 3.13 V and 3.6 V	9, 10, 11		1.5	
		A Port = B Port, 3.3 V operation C_L = 40 pF	02, 03, 04, 05, 06, 07	V_{DD1} = 3.0 V and 3.6 V, V_{DD2} = 3.0 V and 3.6 V	9, 10, 11		1.5	

1/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{DDQ} tests, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. For input terminals not designated, $V_{IN} = V_{SS}$ or $V_{IN} \geq 3.13$ V for device type 01 and 3.0 V for device types 02, 03, 04, 05, 06, 07 and 08.

2/ Temperature range (T_C) for device types 03, 05, and 07 is -40°C to +125°C.

3/ RHA devices supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, this device is only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

4/ This device requires both V_{DD1} and V_{DD2} power supplies for operation. The power supply will be indicated followed by the voltage to which the power supply is set to for the given test.

5/ For negative and positive voltage and current values, the sign designates the potential difference in reference to V_{SS} and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

6/ Guaranteed; tested on a sample of pins per device at 3.6 V, 4.5 V, and 5.5 V. Tested on all pins at 3.13 V for device type 01 and 3.0 V for device types 02, 03, 04, 05, 06, and 07.

7/ Guaranteed; tested on a sample of pins at 3.6 V. Tested on all pins at 5.5 V.

8/ This parameter is unaffected by the state of $\overline{\mathrm{OEx}}$ or DIRx.

9/ Guaranteed; tested on a sample of pins at 3.13 V for device type 01 and 3.0 V for device types 02, 03, 04, 05, 06, and 07 tested on all pins at 4.5 V.

10/ Guaranteed; tested on a sample of pins at 3.13 V for device type 01 and 3.0 V for device types 02, 03, 04, 05, 06, and 07.

11/ Guaranteed based on characterization data but not tested.

12/ This parameter is supplied as design limit but not guaranteed or tested.
13/ No more than one output should be shorted at a time for a maximum duration of one second.
14/ Power does not include power contribution of any CMOS output sink current.
15/ Power dissipation specified per switching output.
16/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 3 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}$(min) + 20%, - 0%, $V_{IL} = V_{IL}$(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices are guaranteed to V_{IH}(min) and V_{IL}(max).
17/ For propagation delay tests, all paths must be tested.
18/ Guaranteed by design but not tested.
19/ Output skew is defined as a comparison of any two transitions high-to-low versus high-to-low and low-to-high versus low-to-high at the same temperature and voltage.
20/ Differential skew is defined as a comparison of any two output transitions high-to-low versus low-to-high and low-to-high versus high-to-low.
21/ For device types 01, 02, 03 04, 05, 06, 07 output skew is defined as a comparison of any two output transitions of the same type at the same temperature and voltage for the same port within the byte:1A1 through 1A8 are compared high-to-low versus high-to-low and low-to-high versus low-to-high; similarly 1B1 through 1B8 are compared, 2A1 through 2A8 are compared and 2B1 through 2B8 are compared.
22/ For device types 01, 02, 03 04, 05, 06, 07 differential output skew is defined as a comparison of any two output transitions of opposite types at the same temperature and voltage for the same port within the byte:1A1 through 1A8 are compared high-to-low versus low-to-high; similarly 1B1 through 1B8 are compared, 2A1 through 2A8 are compared and 2B1 through 2B8 are compared.

TABLE IB. SEP test limits. 1/ 2/

Device type	V_{DD1} = 4.5 V		Bias for latch-up test
	Effective LET no upsets [MeV/(mg/cm^2)]	Maximum device cross section	V_{DD1} = 5.5 V no latch-up 3/ 4/
01 - 05	LET≤ 80	6 x 10^{-9} cm^2/bit 5/	LET ≤ 120
06, 07	LET ≤ 80	6 x 10^{-9} cm^2/bit 5/	LET ≤ 114
08	LET ≤ 64	6/	LET ≤ 111

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Operating temperature is T_A = +125°C ±10°C for SEL and T_A = +25°C±10°C for SEU test.
4/ Tested to a LET = 120 MeV/(mg/cm^2) for device types 01-05, LET = 114 MeV/(mg/cm^2) for device types 06-07 and LET= 111 MeV/(mg/cm^2) for device type 08 with no latch-up (SEL).
5/ The bit error cross section is established from a "hard" D flip-flop that is based on the Weibull distribution from SEU testing, and is performed on the Standard Evaluation Circuit (SEC).
6/ Tested to LET = 80 MeV/(mg/cm^2) for device types 01-07 and LET = 64 MeV/(mg/cm^2) for device type 08 with no single event upsets (SEU).

”

Case outline X

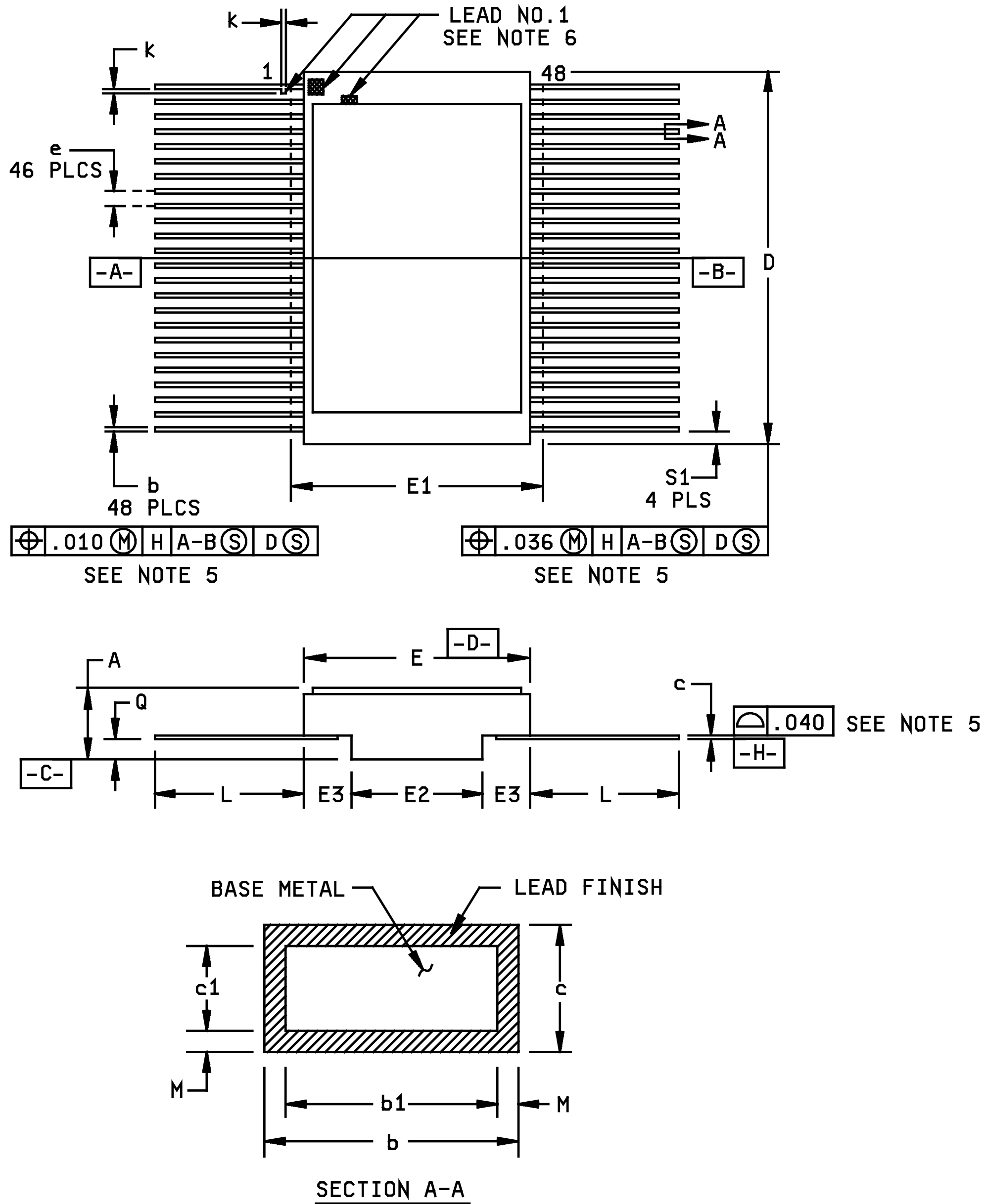


FIGURE 1. Case outline

Case outline X						
	Inches			Millimeters		
Symbol	Min	Nom	Max	Min	Nom	Max
A	.080		.120	2.032		3.048
b	.006		.015	0.1524		0.381
b1	.006		.013	0.1524		0.3302
c	.004		.010	0.1016		0.254
c1	.004		.008	0.1016		0.2032
D	.610		.640	15.494		16.256
E	.370		.390	9.398		9.906
E1	.430		.470	10.922		11.938
E2	.180			4.572		
E3	.030			0.762		
e	.025 BSC			0.635		
k	N/A			N/A		
L	.250		.370	6.35		9.398
Q	.026		.045	0.6604		1.143
S1	.005			0.127		
M			.0015			0.0381
N	48			48		

NOTES:
1. All exposed metalized areas must be gold plated over electroplated nickel per MIL-PRF-38535.
2. The lids are electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Dimension symbology is in accordance with MIL-PRF-38535.
5. Lead position and coplanarity are not measured.
6. ID mark symbol is vendor option: No alpha numeric. One or both ID methods may be used for pin 1 ID.

FIGURE 1. Case outline - Continued.

Case outline Y

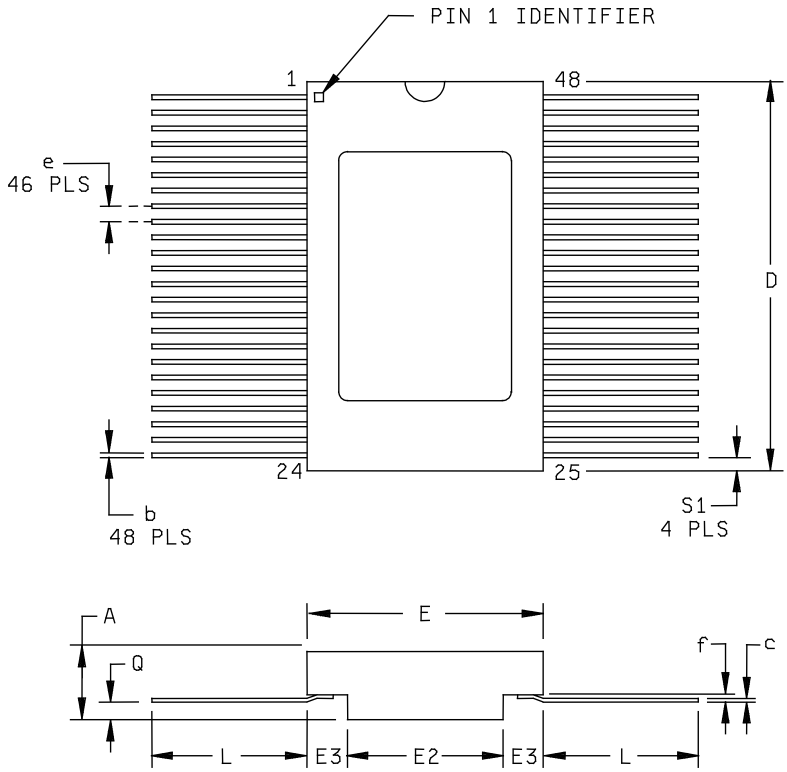


FIGURE 1. Case outline - Continued.

Dimensions				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.086	.107	2.18	2.72
b	.008	.012	0.20	0.30
c	.005	.007	0.12	0.18
D	.613	.627	15.57	15.92
E	.375	.385	9.52	9.78
E2	.245	.255	6.22	6.48
E3	.060	.070	1.52	1.78
e	.025 BSC		0.635 BSC	
f	.008 BSC		0.20 BSC	
L	.270	.370	6.85	9.40
Q	.026	.036	0.66	0.92
S1	.010	.024	0.25	0.61
N	48		48	

FIGURE 1. Case outline - Continued.

Device type	All		
Case outline	X and Y		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DIR1	25	$\overline{OE2}$
2	1B1	26	2A8
3	1B2	27	2A7
4	V_{SS}	28	V_{SS}
5	1B3	29	2A6
6	1B4	30	2A5
7	V_{DD1}	31	V_{DD2}
8	1B5	32	2A4
9	1B6	33	2A3
10	V_{SS}	34	V_{SS}
11	1B7	35	2A2
12	1B8	36	2A1
13	2B1	37	1A8
14	2B2	38	1A7
15	V_{SS}	39	V_{SS}
16	2B3	40	1A6
17	2B4	41	1A5
18	V_{DD1}	42	V_{DD2}
19	2B5	43	1A4
20	2B6	44	1A3
21	V_{SS}	45	V_{SS}
22	2B7	46	1A2
23	2B8	47	1A1
24	DIR2	48	$\overline{OE1}$

Pin description	
Terminal symbol	Description
$\overline{OEx}$ (x = 1, 2)	Output enable inputs (active low)
DIRx (x = 1, 2)	Direction control inputs
mAn (m = 1, 2; n = 1 to 8)	Side A inputs or three-state outputs (3.3 V Port)
mBn (m = 1, 2; n = 1 to 8)	Side B inputs or three-state outputs (5.0 V Port)

FIGURE 2. Terminal connections.

For device types 01, 02, 03, 04 05 and 08.

Inputs		Operation
Enable $\overline{OEx}$	Direction DIRx	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = High voltage level
L = Low voltage level
X = Irrelevant

Port A	Port B	Operation
3.3 Volts	5.0 Volts	Voltage Translator
5.0 Volts	5.0 Volts	Non-Translating
3.3 Volts	3.3 Volts	Non-Translating
V_{SS}	V_{SS}	Cold Spare
3.3 V or 5.0 V	V_{SS}	Port B Cold Spare

NOTE:

Control signals DIRx and $\overline{OEx}$ are 5 volt tolerant inputs. When V_{DD2} is at 3.3 volts, either 3.3 or 5.0 volt CMOS logic levels can be applied to all control inputs. For proper operation, connect power to all V_{DD} and ground all V_{SS} pins (i.e., no floating V_{DD} or V_{SS} input pins). Tie unused inputs to V_{SS}.

If V_{DD1} and V_{DD2} are not powered up together, then V_{DD2} should be powered up first for proper control of DIRx and $\overline{OEx}$. The internal state of DIRx and $\overline{OEx}$ is unknown when V_{DD2} is not powered, because the internal circuitry for these pins is powered by V_{DD2}. Until V_{DD2} reaches 2.75 V $\pm$5% (for device types 01-07) and until V_{DD2} reaches 2.2 V for device type 08, control of the outputs by DIRx and $\overline{OEx}$ cannot be guaranteed. During operation of the part, after power up, insure $V_{DD1} \geq V_{DD2}$.

FIGURE 3. Truth table.

For device types 06 and 07.

Inputs		Operation
Enable $\overline{OEx}$	Direction DIRx	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = High voltage level
L = Low voltage level
X = Irrelevant

Port A	Port B	Operation
3.3 Volts	5.0 Volts	Voltage Translator
5.0 Volts	5.0 Volts	Non-Translating
3.3 Volts	3.3 Volts	Non-Translating
V_{SS}	V_{SS}	Cold Spare
3.3 V or 5.0 V	V_{SS}	Port A Warm Spare
V_{SS}	3.3 V or 5.0 V	Port B Warm Spare

NOTE:

All inputs are 5 volt tolerant. When V_{DD2} is at 3.3 volts, either 3.3 or 5 volt CMOS logic levels can be applied to all control inputs. It is recommended that all unused inputs be tied to V_{SS} through a 1KΩ resistor.
Input signal transitions should be driven to the UT54ACS164245SEI with a rise and fall time that is < 100 ms.

For proper operation, connect power to all V_{DD} pins and ground all V_{SS} pins (ie., no floating V_{DD} or V_{SS} input pins). By virtue of the UT54ACS164245SEI warm spare feature, power supplies V_{DD1} and V_{DD2} may be applied to the device in any order. To ensure the device is in cold spare mode, both supplies, V_{DD1} and V_{DD2} must be equal to V_{SS} ±0.3 V. Warm space operation is in effect when one power supply is > 1.0 V and the other power supply is equal to V_{SS} ±0.3 V. If V_{DD1} has a power on ramp longer than 1 second, then V_{DD2} should be powered on first to ensure proper control of DIRx and $\overline{OEx}$. During normal operation of the part, after power-up, ensure $V_{DD1} \geq V_{DD2}$.

By definition, warm sparing occurs when half of the chip receives its normal V_{DD} supply value while the V_{DD} supplying the other half of the chip is set to 0.0 V. When the chip is “warm spared”, the side that has V_{DD} set to normal operation value is “actively” tri-stated because the chip’s internal OE signal is forced low.
The side of the chip that has V_{DD} set to 0.0 V is “passively” tri-stated by the cold spare circuitry. In order to minimize transients and current consumption, the user is encouraged to first apply a high level to the $\overline{OEx}$ pins and then power down the appropriate supply.

FIGURE 3. Truth table - Continued.

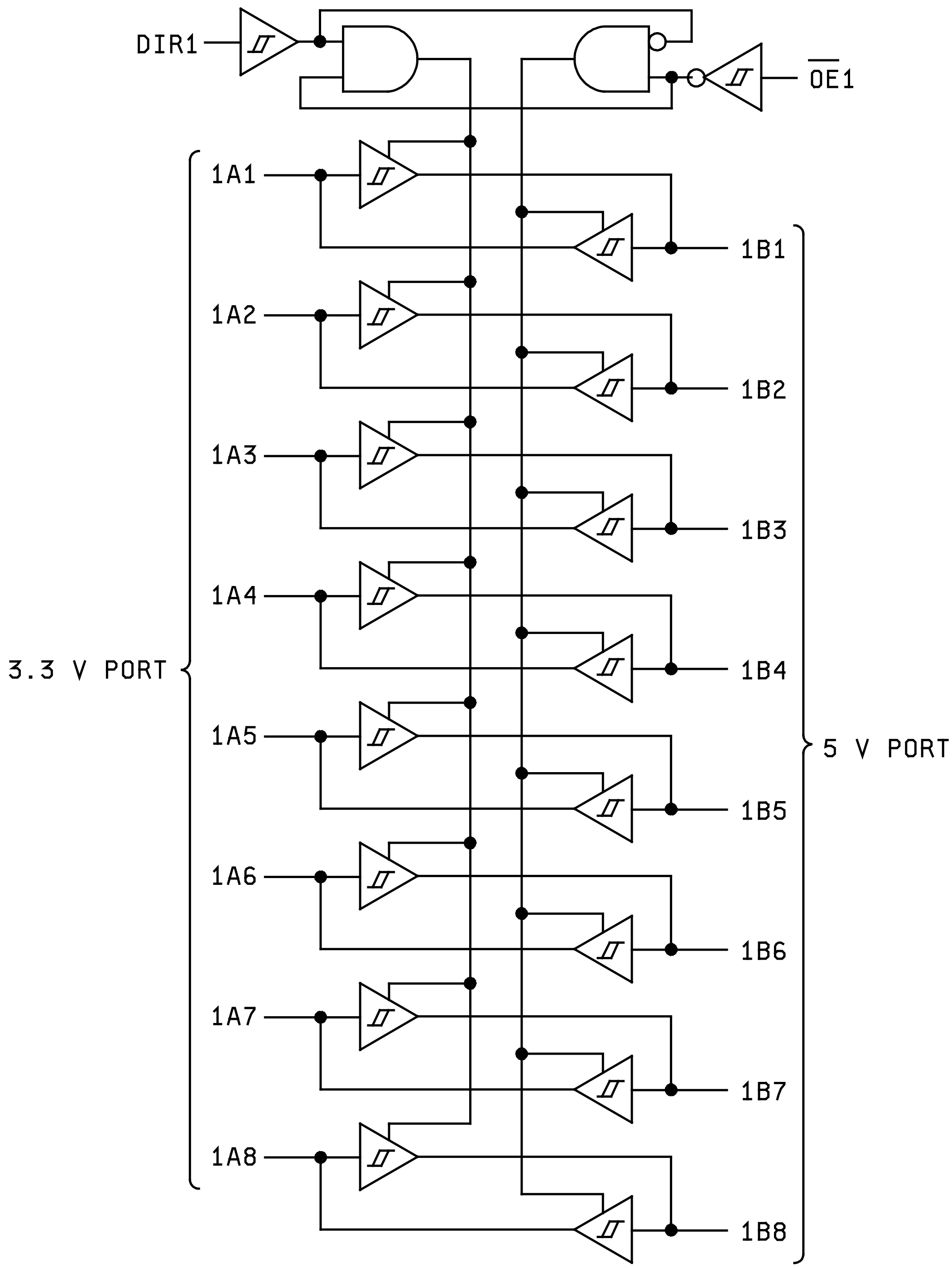


FIGURE 4. Logic diagram.

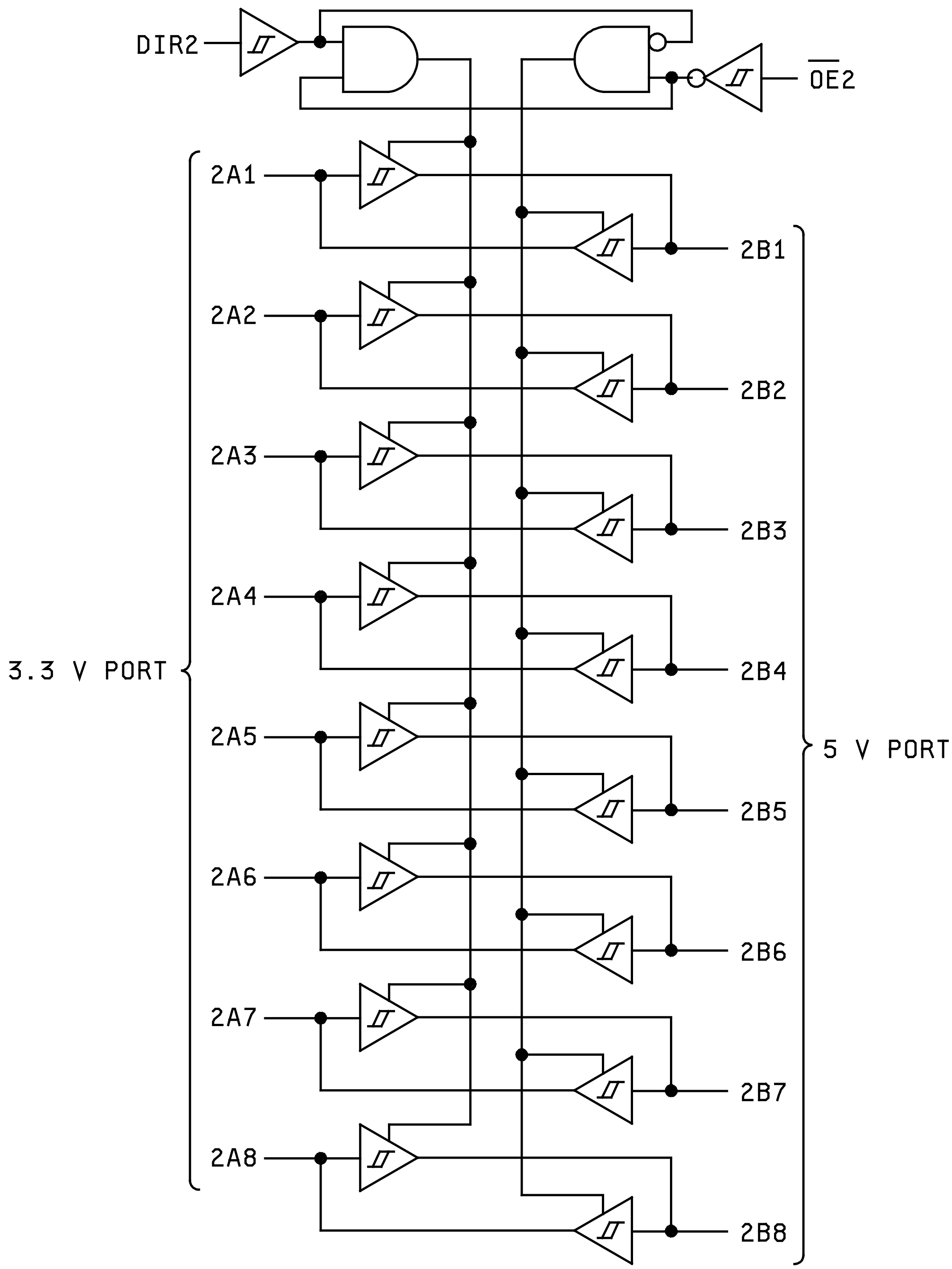


FIGURE 4. Logic diagram - Continued.

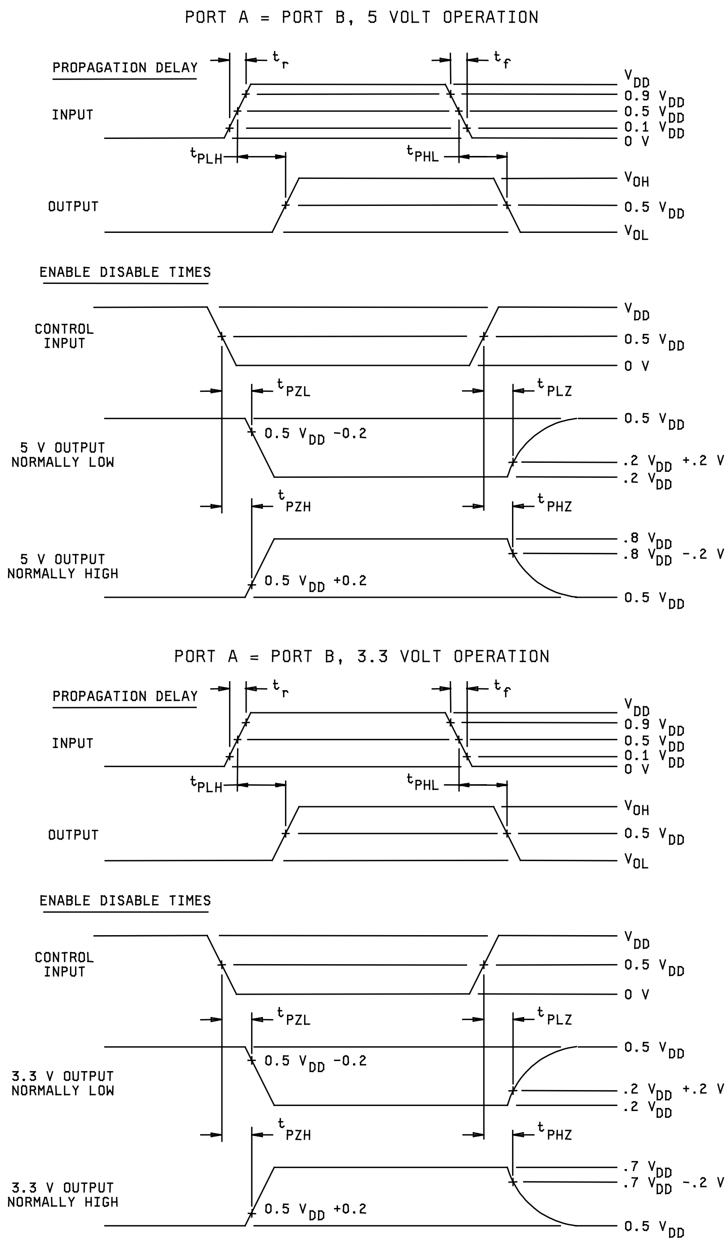
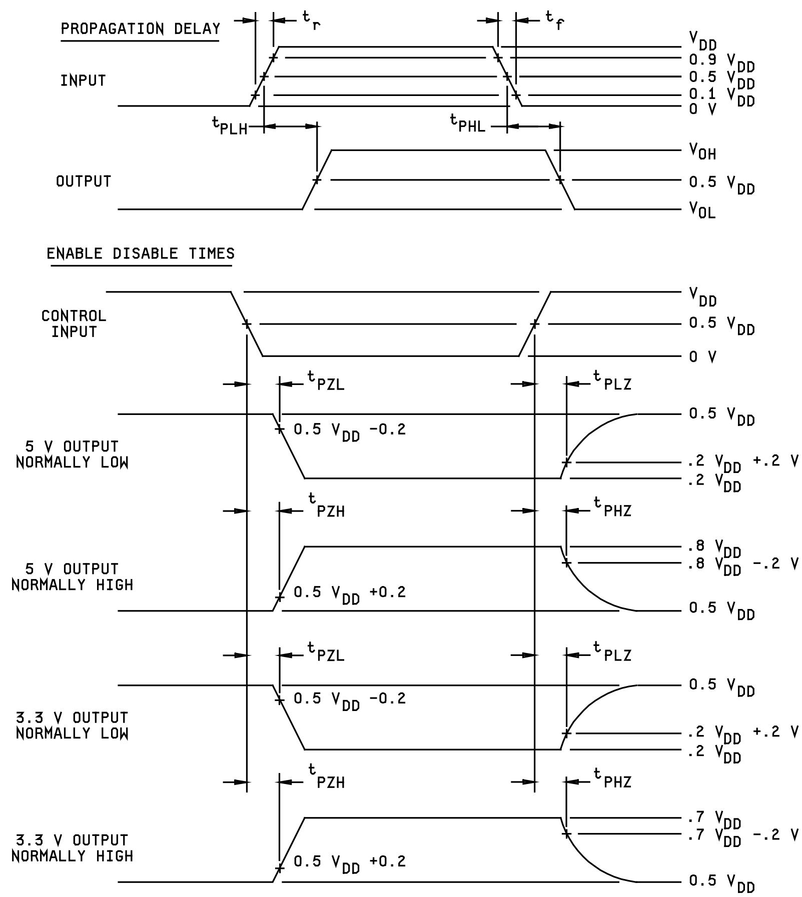
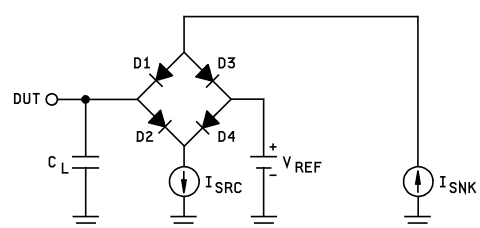


FIGURE 5. Switching waveforms and test circuit.

PORT B = 5 VOLT, PORT A = 3.3 VOLT





TEST CIRCUIT A or EQUIVALENT

NOTES:

1. $V_{REF} = 0.5V_{DD}$.
2. C_L = 40 pF minimum or equivalent (includes test jig and probe capacitance) for device type 01 to 07 and C_L = 50 pF minimum or equivalent for device type 08.
3. I_{SRC} is set to -1.0 mA and I_{SNK} is set to 1.0 mA for t_{PHL} and t_{PLH} measurements.
4. Input signal from pulse generator: V_{IN} = 0.0 V to V_{DD}; f $\leq$ 10 MHz; t_r = 1.0 ns/V $\pm$0.3 ns/V; t_f = 1.0 ns/V $\pm$0.3 ns/V; t_r and t_f shall be measured from 0.1 V_{DD} to 0.9 V_{DD} and from 0.9 V_{DD} to 0.1 V_{DD}, respectively.
5. Equivalent test circuit means that DUT performance will be correlated and remain guaranteed to the applicable test circuit, above, whenever a test platform change necessitates a deviation from the applicable test circuit.

FIGURE 5. Switching waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} and C_{OUT} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz. For C_{IN} and C_{OUT}, test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 3/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	3/ 1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 2, 3, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroups 1 and 7.
2/ PDA applies to subgroups 1, 7, and deltas.
3/ Delta limits, as specified in table IIB herein, shall be required where specified, and the delta values shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameters	Symbol	Delta limits for device types 01 - 05	Delta limits for device types 06, 07 and 08
Output voltage low	V_{OL}	±100 mV	±100 mV
Output voltage high	V_{OH}	±100 mV	±100 mV
Quiescent supply current	I_{DDQ}	Not applicable	±10% or 10 μA whichever is greater

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing testing. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. When required by the customer, dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test 4 devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C for the upset measurements and the maximum rated operating temperature ±10°C for the latchup measurents.

f. Bias conditions shall be V_{DD} = 4.5 V dc for the upset measurements and V_{DD} = 5.5 V dc for the latchup measurements.

g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime, when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA test conditions (SEP).

b. Number of upsets (SEU).

c. Number of transients (SET).

d. Occurrence of latch-up (SEL).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-98580

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

A.1.2 PIN. The PIN shall be as shown in the following example:

```
 5962          R       98580         01           V            9            A
   |           |                     |            |            |            |
Federal       RHA                  Device       Device        Die          Die
stock class   designator           type         class         code         details
designator    (see A.1.2.1)        (see A.1.2.2) designator                (see A.1.2.4)
 \__________  __________/                        (see A.1.2.3)
            V
     Drawing number
```

A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACS164245S	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs and cold sparing
02	54ACS164245S 1/	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs, cold sparing, and extended voltage range
03	54ACS164245S 1/ 2/	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs, cold sparing, extended voltage range, and extended industrial temperature range of -40°C to +125°C
04	54ACS164245SE 1/	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs, cold sparing, extended voltage range, and enhanced AC's
05	54ACS164245SE 1/ 2/	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs, cold sparing, extended voltage range, extended industrial temperature range of -40°C to +125°C, and enhanced AC's
06	54ACS164245SEI 1/	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs, cold sparing, warm sparing, extended voltage range, enhanced AC's and improved power management
07	54ACS164245SEI 1/ 2/	Radiation hardened, Schmitt 16-bit bidirectional multi-purpose transceiver with three-state outputs, cold sparing, warm sparing, extended voltage range, industrial temperature range of -40°C to +125°C, enhanced AC's and improved power management

1/ Device types 02, 03, 04, 05, 06, and 07 have an extended voltage range.
2/ Device types 03, 05, and 07 have an extended industrial temperature range of -40°C to +125°C.

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535.

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01, 02, 03, 04, 05	A-1
06, 07	A-2

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01, 02, 03, 04, 05	A-1
06, 07	A-2

A.1.2.4.3 Interface materials.

Die type	Figure number
01, 02, 03, 04, 05	A-1
06, 07	A-2

A.1.2.4.4 Assembly related information.

Die type	Figure number
01, 02, 03, 04, 05	A-1
06, 07	A-2

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2. APPLICABLE DOCUMENTS

A.2.1 Government specifications, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figures A-1 and A-2.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figures A-1 and A-2.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figures A-1 and A-2.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figures A-1 and A-2.

A.3.2.5 Truth table(s). The truth table(s) shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Irradiation test connections. The irradiation test connections shall be as defined within paragraph 3.2.6 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4. VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer Lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5. DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be in accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6. NOTES

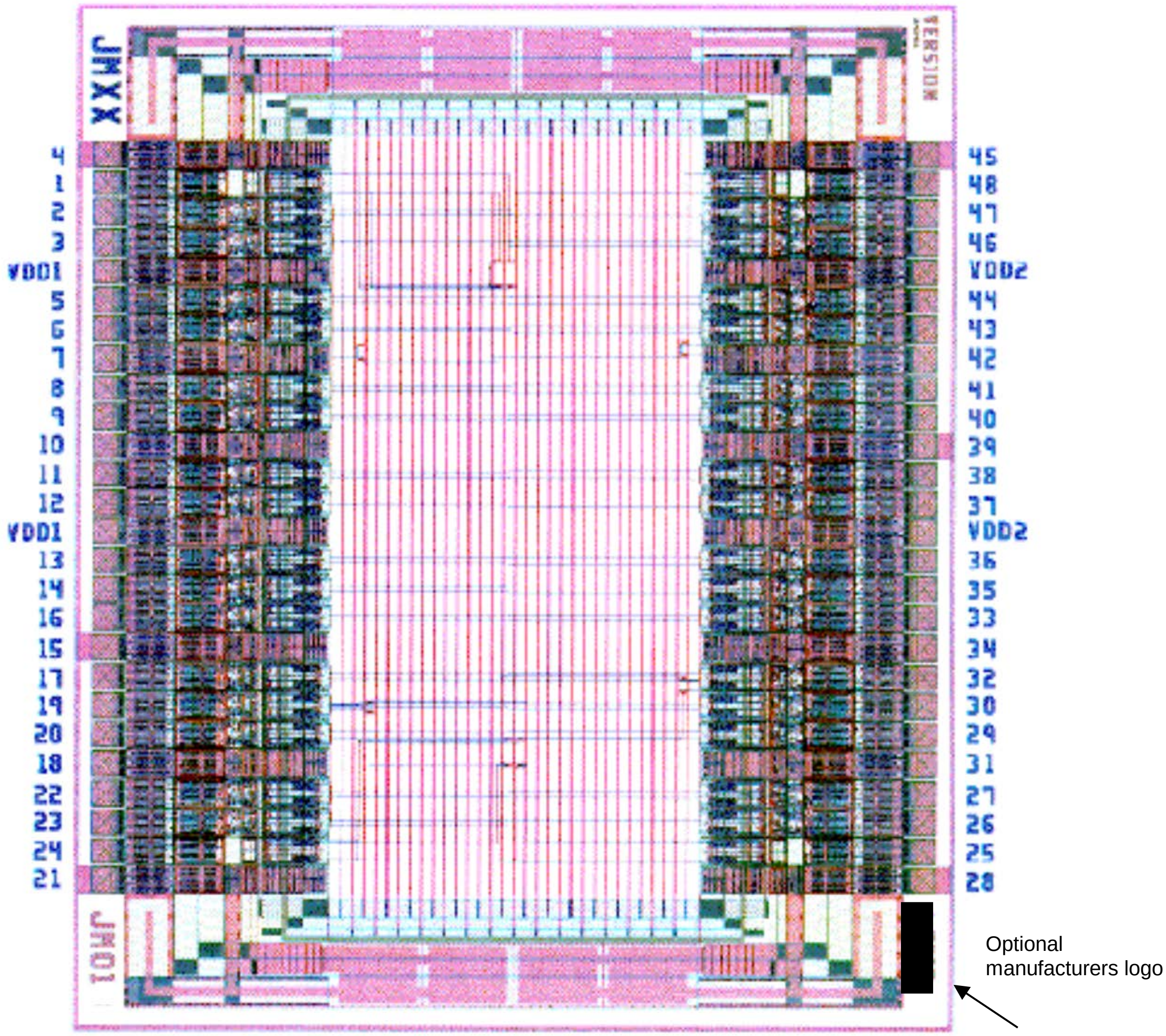
A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, P.O. Box 3990, Columbus, Ohio 43218-3990 or telephone (614) 692-0547.

A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-98580



NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see figure 2).

FIGURE A-1. Die bonding pad locations and electrical functions.

Die physical dimensions.

Die size:	132.97 x 115.827 mils.
Die thickness:	17.5 ±1 mils

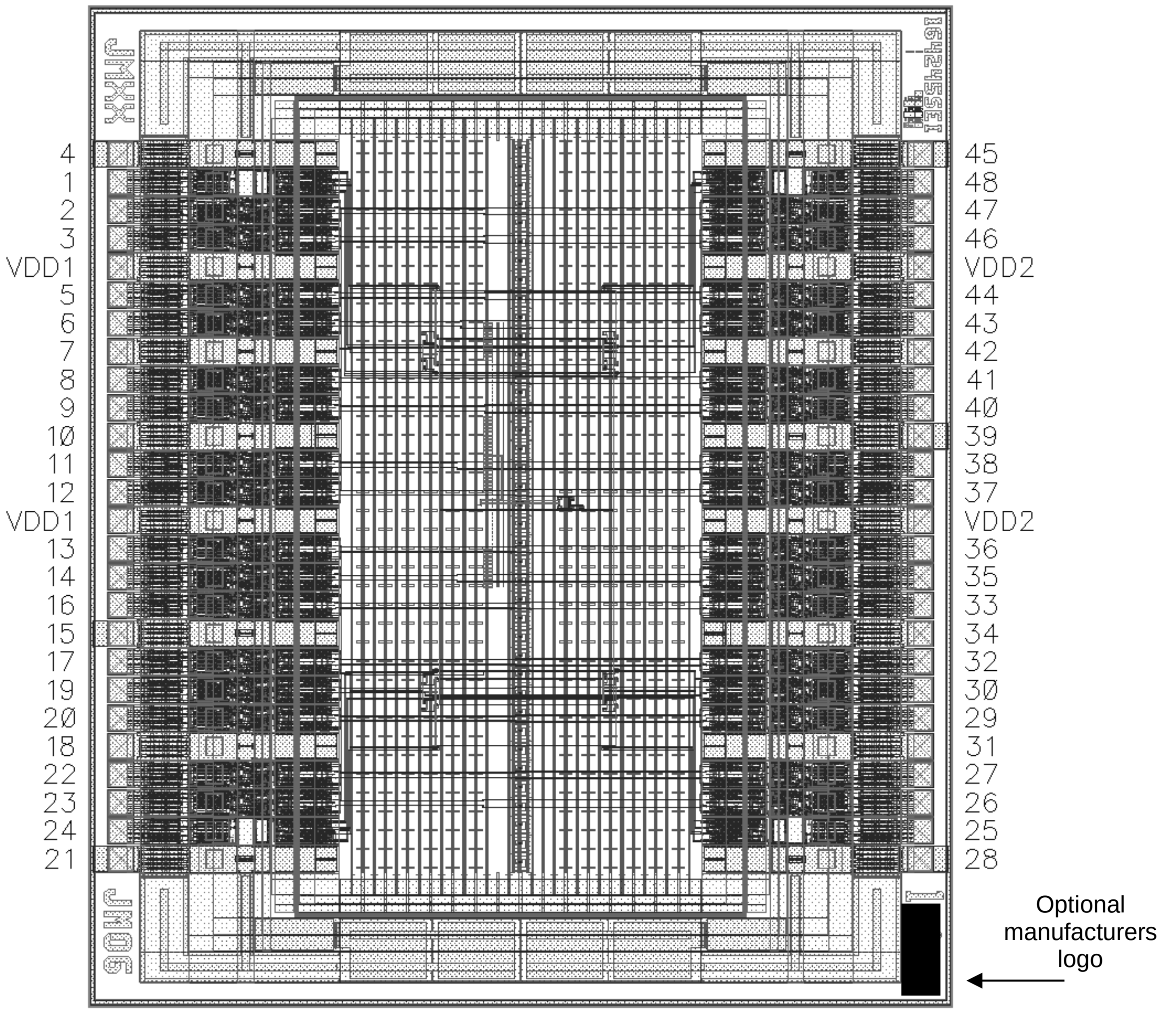
Interface materials.

Top metallization:	Si Al Cu
Thickness:	6.2kÅ – 7.6kÅ
Backside metallization:	None
Glassivation:	
Type:	Oxide/Nitride
Thickness:	9.0kÅ – 11.0kÅ
Substrate:	Epitaxial Layer on Single Crystal Silicon

Assembly related information.

Substrate potential:	Tied to V_{SS}
Special assembly Instructions:	None

FIGURE A-1. Die bonding pad locations and electrical functions – Continued.



NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see figure 2).

FIGURE A-2. Die bonding pad locations and electrical functions.

Die physical dimensions.

Die size:	132.97 x 115.83 mils.
Die thickness:	17.5 ±1 mils

Interface materials.

Top metallization:	Si Al Cu
Thickness:	6.2kÅ – 7.6kÅ
Backside metallization:	None
Glassivation.	
Type:	Oxide/Nitride
Thickness:	9.0kÅ – 11.0kÅ
Substrate:	Epitaxial Layer on Single Crystal Silicon

Assembly related information.

Substrate potential:	Tied to V_{SS}
Special assembly Instructions:	Bond V_{SS} pad first (pins 4, 10, 15, 21, 28, 34, 39 or 45)

FIGURE A-2. Die bonding pad locations and electrical functions – Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-03-10

Approved sources of supply for SMD 5962-98580 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R9858001QXC	65342	UT54ACS164245SUCC
5962R9858001VXC	65342	UT54ACS164245SUCCR
5962R9858001Q9A	65342	UT54ACS164245S-Q DIE
5962R9858001V9A	65342	UT54ACS164245S-V DIE
5962R9858002QXC	65342	UT54ACS164245SUCC 3/
5962R9858002VXC	65342	UT54ACS164245SUCCR 3/
5962R9858002Q9A	65342	UT54ACS164245S-Q DIE 3/
5962R9858002V9A	65342	UT54ACS164245S-V DIE 3/
5962R9858003QXC	65342	UT54ACS164245SUCC 3/ 4/
5962R9858003VXC	65342	UT54ACS164245SUCCR 3/ 4/
5962R9858003Q9A	65342	UT54ACS164245S-Q DIE 3/ 4/
5962R9858003V9A	65342	UT54ACS164245S-V DIE 3/ 4/
5962R9858004QXC	65342	UT54ACS164245SEUCC 3/
5962R9858004VXC	65342	UT54ACS164245SEUCCR 3/
5962R9858004Q9A	65342	UT54ACS164245SE-Q DIE 3/
5962R9858004V9A	65342	UT54ACS164245SE-V DIE 3/

See footnotes at end of table.

DATE: 14-03-10

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R9858005QXC	65342	UT54ACS164245SEUCC 3/ 4/
5962R9858005VXC	65342	UT54ACS164245SEUCCR 3/ 4/
5962R9858005Q9A	65342	UT54ACS164245SE-Q DIE 3/ 4/
5962R9858005V9A	65342	UT54ACS164245SE-V DIE 3/ 4/
5962R9858006QXC	65342	UT54ACS164245SEIUCC 3/
5962R9858006VXC	65342	UT54ACS164245SEIUCCR 3/
5962R9858006Q9A	65342	UT54ACS164245SEI-Q DIE 3/
5962R9858006V9A	65342	UT54ACS164245SEI-V DIE 3/
5962R9858007QXC	65342	UT54ACS164245SEIUCC 3/ 4/
5962R9858007VXC	65342	UT54ACS164245SEIUCCR 3/ 4/
5962R9858007Q9A	65342	UT54ACS164245SEI-Q DIE 3/ 4/
5962R9858007V9A	65342	UT54ACS164245SEI-V DIE 3/ 4/
5962R9858008VYC	F8859	RHRAC164245K01V
5962R9858008QYC	F8859	RHRAC164245K01Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ These parts have an extended voltage range.

4/ These parts have an extended industrial temperature range of -40°C to +125°C.

Vendor CAGE number	Vendor name and address
65342	Aeroflex Colorado Springs, Inc 4350 Centennial Boulevard Colorado Springs, CO 80907-3486
F8859	ST Microelectronics 3 rue de Suisse BP4199 35041 RENNES cedex2 - France

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.